IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A multi-chip-module with a base carrier (1), on which at least in some areas signal conductor tracks (2, 8) arranged at least in a single layer and signal contact surfaces (4) are arranged, and with at least one semiconductor component (11) connected with signal conductor tracks (2) and signal contact surfaces (4) operating in the signal range, wherein additionally on the base carrier (1) at least in some areas power conductor tracks (5) and power contact surfaces (7, 7a) are arranged in at least a single layer, at least one power electronics component (12) operating in the power range is provided, which is connected with at least one power conductor track (5), at least one power contact surface (7, 7a) and at least one signal conductor track (2, 8) and the power conductor tracks (5) have a larger cross section than the signal conductor tracks (2) at least on the basis of greater thickness dimensions.

2. (Amended) The multi-chip-module in accordance with claim 1, wherein the at least one signal conductor track (2, 8) leading to a power electronics component (12) essentially seamlessly verges into a power conductor track (5) and/or power contact surface (7).

3. (Amended) The multi-chip-module according to claim 1, wherein the ratio of the height of a power conductor track (5) and/or power contact surface (7, 7a) to the signal conductor track (2,8) and/or signal contact surface (4) is situated within the range of 2 to 300, in preference 120 to 130.

4. (Amended) The multi-chip-module according to claim 1, wherein the ratio of the conductor cross section of a power conductor track (5) and/or power contact surface (7, 7a) to the conductor cross section of a signal conductor track (2, 8) amounts to 2 to 1000, in preference 80 to 400.

5. (Amended) The multi-chip-module according to claim 1, wherein the ratio of height to width of a power conductor track (5) and/or power contact surface (7, 7a) is situated in the range of 0.1 to 10, in preference 1 to 4.

6. (Amended) The multi-chip-module according to claim 1, wherein at least one power conductor track (5) merges into several power contact surfaces (7a) for the common contacting of a power electronics component (12).

7. (Amended) The multi-chip-module according to claim 1, wherein signal connection contact surfaces (3) and power connection contact surfaces (6) are provided for an external connection belonging to them, wherein the signal connection contact surfaces (3) and the power connection contact surfaces (6) essentially are of the same height.

8. (Amended) The multi-chip-module according to claim 1, wherein signal connection contact surfaces (3) and power connection contact surfaces (6) are arranged on the side of the base carrier (1), which is opposite the semiconductor components (11) and power electronics components (12) (reverse side), wherein the connection contact surfaces (3, 6) are electrically in connection with the opposite side (front side) by means of conductor track sections passing through the base carrier (1).

9. (Amended) The multi-chip-module according to claim 1, wherein the dimension, which results from the height of a power conductor track (5) minus the height of a power contact surface (7a) electrically in connection with this power conductor track (5), is either the same or greater than the height of the power electronics component (12) contacting this power contact surface (7a).

10. (Amended) The multi-chip-module according to claim 1, wherein on the base carrier (1) at least one heat conducting element is jointly arranged, which is in a thermally conducting connection with a power electronics component (12).

11. (Amended) The multi-chip-module according to claim 10, wherein the at least one heat conducting element (9) is connected with a heat exchanger device (13).

12. (Amended) The multi-chip-module according to claim 11, wherein the heat exchanger device (13) is located on the reverse side of the base carrier (1) and the heat conducting element (9) passes through the base carrier (1).

13. (Amended) The multi-chip-module according to claim 11, wherein the heat exchanger device (13) comprises fine cooling ribs with a ratio of height to width of 0.1 to 10, in preference 1 to 4.

14. (Amended) The multi-chip-module according to claim 1, wherein a heat exchanger device (13) is directly thermally conductively connected with a power electronics component (12).

15. (Amended) The multi-chip-module according to claim 1, wherein the signal connection contact surfaces (3) and the power connection contact surfaces (6) are grouped and arranged on the base carrier (1) in such a manner, that the module is capable of being inserted into a standardised base.

16. (Amended) A method for manufacturing a multi-chip-module, comprising the steps of:

preparing a base carrier (1) with signal conductor tracks (2, 8) and signal contact surfaces (4),

depositing a structured layer, by which at least the signal conductor tracks (2) and signal contact surfaces (4) are essentially covered with the exception of connection points and which comprises a negative structure of the power conductor tracks (5) and/or power contact surfaces (7, 7a),

filling-up of the negative structure by means of a metallisation process for the creation of the power conductor tracks (5) and/or power contact surfaces (7), wherein at the connection points a contacting of the signal conductor tracks (2, 8) and/or signal contact surfaces (4) and of the power conductor tracks (5) and/or the power contact surfaces (7) is effected.

17. (Amended) The method according to claim 16, wherein a conductive adhesive layer is deposited on the base carrier (1) in the zone of the negative structure, which serves as base for the metallisation process.

18. (Amended) The method according to claim 16, wherein the structured layer is deposited by means of a photo-lithographic process.

19. (Amended) The method according to claim 16, wherein the metallisation process is effected by the galvanic deposition of metal.

20. (Amended) The method according to claim 19, wherein, following the metallisation process, the structured layer is removed.